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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,093	GILBERT ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/11/06,5/30/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed on April 20, 2006, in response to PTO Office Action mailed on November 16, 2005. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. No claims have been amended, added, or canceled. Claims 1-33 remain pending.

Response to Arguments

3. Applicant's arguments filed April 20, 2006, regarding the rejection of claims 11, 14, 18, 21, 24, and 28 under 35 USC 112, first paragraph, have been fully considered but they are not persuasive.

a. In response to the rejection of claims 11, 14, 18, 21, 24, and 28 under 35 USC 112, first paragraph, Applicant argues on pages 9-10 of the remarks that "there is no requirement that claims use the exact terms used in the specification. Throughout the specification, Applicant use words "inner" and "outer" to describe L1 caches and L2 caches... The phrase "inner relationship" can be inferred from the specification and be readily understood by one of ordinary skill in the art".

i. Examiner respectfully disagrees. Simply because the specification mentions the words "inner" and "outer" in describing L1 and L2 caches does not make the disclosure enabling for the limitation "inner relationship" recited in independent claims 11, 14, 18, 21, 24, and 28. Furthermore, Examiner would like to mention that in the specification an "inner cache" is being referred to as an L1 cache and "outer cache" as an L2 cache. In this case, should Examiner assume that "inner relationship" is being referred to as "L1 relationship"? As such, the evidence provided by Applicant is not sufficient to overcome the rejection for lack of enablement under 35 USC 112, first paragraph.

ii. Additionally, Once the examiner has established a prima facie case of lack of enablement, the burden falls on the Applicant to present persuasive arguments, supported by suitable proofs where necessary, that one skilled in the art would have been able to make and use the claimed invention using the disclosure as a guide. *In re Brandstadter, 484 F.2d 1395, 179 USPQ 286 (CCPA 1973).* Evidence to supplement a specification which on its face appears deficient under 35 USC 112 must establish that the information which must be read into the specification to make it complete would have been known to those of ordinary skill in the art.

4. Applicant's arguments with respect to the 102 rejection of claims 1 and 31 and the 103 rejection of claims 2-30 and 32-33 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) in view of WO 00/52582.

As per claim 1, Arimilli (6,629,268) discloses an apparatus, comprising: a first interface [Fig.2; Bus Interface Unit 35]; a second interface not directly coupled to said first interface [Fig.2; Interface 18]; and a cache accessible from said first interface and said second interface [Fig.2; L2 cache, Bus Interface 35, Interface 19; col.8, lines 6-33].

However, Armilli (268) does not specifically teach a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface as required.

WO 00/52582 discloses a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface [Fig. 1; page 11, ll 16-32; page 12, ll 21-27] to increase the performance capability of processor systems while ensuring that the cache memory block is not read unnecessarily (page 1, ll 1-5; page 11, ll 18-23).

Since the technology for implementing a cache memory system with a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface was well known as evidenced by WO 00/52582, an artisan would have been motivated to implement this feature in the system of Arimilli (268) in order to increase the performance capability of processor systems while ensuring that the cache memory block is not read unnecessarily. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Arimilli (268) to include a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface since this would have increased the performance capability of processor systems while ensuring that the cache memory block is not read unnecessarily (page 1, ll 1-5; page 11, ll 18-23) as taught by WO 00/52582.

As per claim 31, the rationale in the rejection of claim 1 is herein incorporated. Arimilli (268) further discloses a bus bridge to a third interface [Fig.1]; and an input-output device coupled to a third interface [Fig.3].

7. Claims 2-10 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) in view of WO 00/52582 and further in view of Arimilli (2002/0129211).

As per claim 2, Arimilli (268) and WO disclose the claimed invention as discussed above in the previous paragraphs. However, Arimilli (268) and WO do not specifically teach the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor as required by the claims.

Arimilli (2002/0129211) discloses the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor [par. 10] to resolve conflicts between requests to modify a cache line (par. 2).

Since the technology for implementing a cache system with the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor was well known as evidenced by Arimilli (211), an artisan would have been motivated to implement this feature in the system of Arimilli (268) and WO in order to resolve conflicts between requests to modify a cache

line. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Armilli (268) and WO to include the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor because this would have resolved conflicts between requests to modify a cache line (par. 2).

As per claim 3, Arimilli (211) discloses a second cache coherency state is to reduce snoop transactions on said second interface [par. 5].

As per claim 4, Arimilli (211) discloses said first cache coherency state is exclusive and said second cache coherency state is shared [pars. 6, 24 and 36].

As per claim 5, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is shared [par. 8].

As per claim 6, Arimilli (211) discloses second cache coherency state supports speculative invalidation [par. 6].

As per claim 7, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is invalid [par. 7].

As per claim 8, Arimilli (211) discloses first cache coherency state is exclusive

and said second cache coherency state is invalid [pars. 6 and 36].

As per claim 9, Arimilli (211) discloses the first cache coherency state is shared and said second cache coherency state is invalid [par. 7].

As per claim 10, Arimilli (211) discloses the second cache coherency state further supports explicit invalidation [pars. 7 and 10].

As per claim 32, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 33, the rationale in the rejection of claim 3 is herein incorporated.

8. Claims 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (2002/0129211) in view of WO 00/52582.

As per claim 11, Armilli (211) discloses a method, comprising: associating a first cache coherency state with a first cache line in a first cache [par. 10]; associating a second cache coherency state with a second cache line in a second cache in an inner relationship to said first cache [pars. 24 and 29];

However, Arimilli (211) does not specifically teach transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces; and

transitioning a second cache coherency state to a third cache coherency state as required by the claim.

WO 00/52582 discloses transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces [Fig. 3; page 7, ll 27 to page 8, ll 13; page 15; ll 1-19]; and transitioning a second cache coherency state to a third cache coherency state [Fig .3; page 15, ll 15-19] to allow the cache to have a deeper knowledge about the state situation within the processor system, which allows it to relay and/or capture requests directed to the individual processors (page 15, ll 22-25).

Since the technology for implementing a cache system with transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces was well known as evidenced by WO 00/52582, an artisan would have been motivated to implement this feature in the system Arimilli (211) since this would have allowed the cache to have a deeper knowledge about the state situation within the processor system, which allows it to relay and/or capture requests directed to the individual processors. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Arimilli (211) to include transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces in order to the cache to have a deeper knowledge about the state situation within the processor system, which allows it to relay and/or capture requests

directed to the individual processors (page 15, ll 22-25) as taught by WO 00/52582.

As per claim 12, WO 00/52582 discloses a first cache coherency state is exclusive, a second cache coherency state is invalid, and a third cache coherency state is shared [Fig. 3].

As per claim 13, WO 00/52582 discloses a first cache coherency state is modified, said second cache coherency state is modified, and said third cache coherency state is invalid [Fig. 3].

As per claim 14, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 15, Arimilli (211) discloses the first cache coherency state is modified [par. 36].

As per claim 16, Arimilli (211) discloses the first cache coherency state is exclusive [par. 36].

As per claim 17, Arimilli (211) discloses the first cache coherency state is shared [par. 37].

As per claim 18, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 19, WO 00/52582 discloses the first cache coherency state is invalid and the joint cache coherency state is exclusive-shared [Fig. 3].

As per claim 20, WO 00/52582 discloses the first cache coherency state is modified-invalid and the joint cache coherency state is modified-shared [Fig. 3].

As per claim 21, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 22, the rationale in the rejection of claim 12 is herein incorporated.

As per claim 23, the rationale in the rejection of claim 13 is herein incorporated.

As per claim 24, the rationale in the rejection of claim 14 is herein incorporated.

As per claim 25, the rationale in the rejection of claim 15 is herein incorporated.

As per claim 26, the rationale in the rejection of claim 16 is herein incorporated.

As per claim 27, the rationale in the rejection of claim 17 is herein incorporated.

As per claim 28, the rationale in the rejection of claim 18 is herein incorporated.

As per claim 29, the rationale in the rejection of claim 19 is herein incorporated.

As per claim 30, the rationale in the rejection of claim 20 is herein incorporated.

Conclusion

9. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 5/11/06 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art

disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Mano Padmanabhan 7/10/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 10, 2006

Mardochee Chery
Examiner
AU: 2188